



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : William R. Wheeler et al.
Serial No.: 09/941,952
Filed : August 29, 2001
Assignee : Intel Corporation
Title : SIMULATING A LOGIC DESIGN

Art Unit: 2123
Examiner:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Office action on the merits. No fee is required.

The documents are in the English language; hence no concise
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Applicant : William R. Wheeler et al.
Serial No.: 09/941,952
Filed : August 29, 2001


Attorney's Docket No.:10559-597001

Examiner's initials in the left column per MPEP 609 are
earnestly solicited along with an early action on the merits.

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Respectfully submitted,

Date: 3/12/04



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Substitute Form PTO-1449 (Modified) Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-597001	Application No. 09/941,952
	Applicant William R. Wheeler et al.		
	Filing Date August 29, 2001	Group Art Unit 2123	

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	RE 38,059	04/2003	Yano, et al.			
	AB	4,703,435	10/1987	Darringer, et al.			
	AC	4,970,664	11/1990	Kaiser, et al.			
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Examiner Signature				Date Considered			
EXAMINER: Initials citation considered. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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Sheet 3 of 4Substitute Form PTO-1449
(Modified)U.S. Department of Commerce
Patent and Trademark OfficeAttorney's Docket No.
10559-597001Application No.
09/941,952**Information Disclosure Statement
by Applicant**

(Use several sheets if necessary)

(37 CFR §1.98(b))

Applicant
William R. Wheeler et al.Filing Date
August 29, 2001Group Art Unit
2123**U.S. Patent Documents**

Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
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	AZZZ	WO 98/55879	12/1998	WIPO				

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							Yes	No
U	AAAAA	WO 99/39268	08/1999	WIPO				
"	ABBBB	WO 00/65492	11/2000	WIPO				

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
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	AEEEE	Lahti, et al., "SADE: a Graphical Toll for VHDL-Based System Analysis", 1991 IEEE International Conference on Computer-Aided Design, November 11, 1991, pp. 262-265.
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	AGGGG	NB84035598, "Binary Relational Schema to Model Structured LSI Design", IBM Technical Disclosure Bulletin, Vol. 26, No. 10B, March 1984, pp. 5598-5601.
	AHHHH	NN7807629, "Functional Oriented Symbolic Macromodeling Algorithm", IBM Technical Disclosure Bulletin, Vol. 21, No. 2, July 1978, pp. 629-631.
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"	AMMMM	Yli-Pietila, et al., "The Design and Simulation of Complex Multitechnology Systems", IEEE International Conference on Systems Engineering, August 9, 1990, pp. 474-477.

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